Clean Version of Amended Specification Paragraphs

Title: ON-CHIP SUBSTRATE REGULATOR TEST MODE
Applicant: Gary R. Gilliam
Serial No.: 09/935,086

The paragraph beginning on page 2, line 24:

In one embodiment of Figure 1, a memory device 100 is shown having a number of memory cells 110. The invention is, however not limited to embodiments that include a memory device. Referring to Figure 1, Vcc is a supply voltage level. An n-channel MOSFET MI, has its gate coupled its drain. The drain of Ml and the gate of MI are coupled to the supply voltage level Vcc. An n-channel MOSFET M2, has its gate coupled to its drain. The gate and drain of M2 are coupled to the source of MI. An n-channel MOSFET M3, has its gate coupled to its drain. The gate of M3 and the drain of M3 are coupled to the source of M2. An n-channel MOSFET M41 has its drain coupled to the drain of M3. The source of M4 is coupled to the source of M3. The gate of M4 is coupled to be controlled by a control voltage level ENl. An n-channel MOSFET M5, has its gate coupled to the gate of M3. The drain of M5 is coupled to the source of M3. The source of M5 is coupled to a substrate node Vbb. An n-channel MOSFET M6, has its drain coupled to the drain of M5. The source of M6 is coupled to the source of M5 and to the substrate node Vbb. The gate of M6 is coupled to be controlled by a control voltage level EN2. The substrate node Vbb, is coupled to the substrate of a integrated circuit chip on which the substrate voltage regulator circuit is contained.

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Clean Version of Pending Claims

ON-CHIP SUBSTRATE REGULATOR TEST MODE
Applicant: Gary R. Gilliam
Serial No.: 09/935,086

Claims 23-47, as of November 25, 2002 (date of response to first office action filed).

23. A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to at least one diode in the series of diodes for electrically bypassing at least one diode.

24. The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling a plurality of bypass transistors to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

25. The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one bypass transistor to plurality of diodes for electrically bypassing the plurality of diodes.

26. The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one normally off bypass transistor to at least one diode leaving the at least one diode unbypassed during normal operation and allowing the at least one diode to be selectively bypassed during testing operations.

27. The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one normally on bypass transistor to at least one diode leaving the at least one diode bypassed during normal operation and allowing the at least one diode to be selectively unbypassed during testing operations.

28. A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

29. The method of claim 28 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally off bypass transistor to a plurality of diodes leaving the plurality of diodes unbypassed during normal operation and allowing the plurality of diodes to be selectively bypassed during testing operations.

30. The method of claim 28 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally on bypass transistor to a plurality of diodes leaving the plurality of diodes bypassed during normal operation and allowing the plurality of diodes to be selectively unbypassed during testing operations.

31 A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate

voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling a plurality of bypass transistors to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

32. The method of claim 31 wherein coupling a plurality of bypass transistors to a plurality of diodes includes coupling a plurality of normally off bypass transistors to a plurality of diodes leaving the plurality of diodes unbypassed during normal operation and allowing the plurality of diodes to be selectively bypassed during testing operations.

33. The method of claim 31 wherein coupling a plurality of bypass transistors to a plurality of diodes includes coupling a plurality of normally on bypass transistors to a plurality of diodes leaving the plurality of diodes bypassed during normal operation and allowing the plurality of diodes to be selectively unbypassed during testing operations.

34. A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling at least one bypass transistor to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing at least one diode connected transistor.

35. The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one bypass transistor to plurality of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

36. The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one normally off bypass transistor to at least one diode connected transistor leaving the at least one diode connected transistor unbypassed during normal operation and allowing the at least one diode connected transistor to be selectively bypassed during testing operations.

37. The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one normally on bypass transistor to at least one diode connected transistor leaving the at least one diode connected transistor bypassed during normal operation and allowing the at least one diode connected transistor to be selectively unbypassed during testing operations.

38. A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

39. The method of claim 38 wherein coupling at least one bypass transistor to a plurality of diode connected transistors includes coupling a plurality of bypass transistors to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

40. The method of claim 38 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally off bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors unbypassed during normal operation and allowing the plurality of diode connected transistors to be selectively bypassed during testing operations.

41. The method of claim 38 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally on bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors bypassed during normal operation and allowing the plurality of diode connected transistors to be selectively unbypassed during testing operations.

42. A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling a plurality of bypass transistors to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

43. The method of claim 42 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally off bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors unbypassed during normal operation and allowing the plurality of diode connected transistors to be selectively bypassed during testing operations.

44. The method of claim 42 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally on bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors bypassed during normal operation and allowing the plurality of diode connected transistors to be selectively unbypassed during testing operations.

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45. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diodes in the series of diodes for electrically bypassing a portion of the plurality of diodes.

46. (New) The method of claim 45 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally off bypass transistor to a plurality of diodes leaving the portion of the plurality of diodes unbypassed during normal operation and allowing the portion of the plurality of diodes to be selectively bypassed during testing operations.

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47. (New) The method of claim 45 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally on bypass transistor to a plurality of diodes leaving the portion of the plurality of diodes bypassed during normal operation and allowing the portion of the plurality of diodes to be selectively unbypassed during testing operations.